WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a semiconductor substrate having source and drain regions located therein and having similar doping profiles;

a channel region extending from said source region to said drain region;

a dielectric layer located over said source and drain regions and having first and second thicknesses wherein said second thickness is substantially less than said first thickness and is partially located over said channel region; and

a gate located over said dielectric layer wherein said second thickness is located between an end of said gate and one of said source and drain regions.

2. The semiconductor device recited in Claim 1 wherein said first thickness ranges between about 25 nm to about 50 nm.

3. The semiconductor device recited in Claim 1 wherein said second thickness ranges between about 6 nm and about 20 nm.

4. The semiconductor device recited in Claim 1 wherein said dielectric layer includes an interface between first and second layers thereof.

5. The semiconductor device recited in Claim 1 wherein said doping profiles of said source and drain regions include a doping concentration of about 1.0E20 atoms/cm^3.

6. The semiconductor device recited in Claim 1 wherein said source and drain regions each include a lightly doped region, wherein said end of said gate and said second thickness are located over one of said lightly doped regions.

7. The semiconductor device recited in Claim 6 wherein said lightly doped regions have a doping concentration ranging between about 1.0E17 atoms/cm^3 and about 1.0E18 atoms/cm^3.

8. The semiconductor device recited in Claim 1 wherein said gate is a floating gate and said device further includes a control gate located over said floating gate.

9. The semiconductor device recited in Claim 1 wherein a coupling ratio of said semiconductor device is at least about 0.7.

10. A method of manufacturing a semiconductor device, comprising:

implanting source and drain regions having similar doping profiles in a semiconductor substrate, thereby defining a channel region extending from said source region to said drain region;

locating a dielectric layer over said source and drain regions, said dielectric layer having first and second thicknesses wherein said second thickness is substantially less than said first thickness and is partially located over said channel region; and

forming a gate over said dielectric layer wherein said second thickness is located between an end of said gate and one of said source and drain regions.

11. The method recited in Claim 10 wherein said implanting includes implanting said source and drain regions simultaneously.

12. The method recited in Claim 10 wherein said first thickness ranges between about 25 nm to about 50 nm.

13. The method recited in Claim 10 wherein said second thickness ranges between about 6 nm and about 20 nm.

14. The method recited in Claim 10 wherein said locating includes forming an interface between first and second layers of said dielectric layer.

15. The method recited in Claim 10 wherein said implanting includes implanting said source and drain regions to a concentration of about 1.0E20 atoms/cm^3.

16. The method recited in Claim 10 wherein said implanting includes implanting a lightly doped region in each of said source and drain regions, wherein said end of said gate and said second thickness are located over one of said lightly doped regions.

17. The method recited in Claim 16 wherein said implanting said lightly doped region includes implanting to a concentration ranging between about 1.0E17 atoms/cm^3 and about 1.0E18 atoms/cm^3.

18. The method recited in Claim 10 wherein said gate is a floating gate and further including forming a control gate over said floating gate.

19. An integrated circuit, comprising:

transistors formed over or in a semiconductor substrate;

memory cells, including:

source and drain regions located in said semiconductor substrate and having similar doping profiles;

a channel region extending from said source region to said drain region;

a dielectric layer located over said source and drain regions and having first and second thicknesses wherein said second thickness is substantially less than said first thickness and is partially located over said channel region; and

a gate located over said dielectric layer wherein said second thickness is located between an end of said gate and one of said source and drain regions; and

interconnects connecting said transistors and said memory cells to form an integrated circuit.

20. The integrated circuit recited in Claim 19 wherein said memory cells are EEPROM cells.

21. The integrated circuit recited in Claim 19 wherein said first thickness ranges between about 25 nm to about 50 nm and said second thickness ranges between about 6 nm and about 20 nm.

22. The integrated circuit recited in Claim 19 wherein a coupling ratio of each of said memory cells is at least about 0.7.

23. The integrated circuit recited in Claim 19 wherein said source and drain regions each include a lightly doped region, wherein said end of gate and said second thickness are located over one of said lightly doped regions.

24. The integrated circuit recited in Claim 19 wherein said source and drain regions include a doping concentration of about 1.0E20 atoms/cm^3 and said memory cells further include lightly doped regions have a doping concentration ranging between about 1.0E17 atoms/cm^3 and about 1.0E18 atoms/cm^3.